

74AHC74; 74AHCT74

Dual D-type flip-flop with set and reset; positive-edge trigger

Rev. 8 — 22 April 2020

Product data sheet

1. General description

The 74AHC74; 74AHCT74 is a high-speed Si-gate CMOS device and is pin compatible with Low-Power Schottky TTL (LSTTL). It is specified in compliance with JEDEC standard No. 7-A.

The 74AHC74; 74AHCT74 is a dual positive-edge triggered, D-type flip-flop with individual data inputs (D), clock inputs (CP), set inputs (\overline{SD}) and reset inputs (\overline{RD}). It also has complementary outputs (Q and \overline{Q}).

The set and reset are asynchronous active LOW inputs that operate independent of the clock input. Information on the data input is transferred to the Q output on the LOW to HIGH transition of the clock pulse. The data inputs must be stable one set-up time prior to the LOW to HIGH clock transition for predictable operation.

Schmitt-trigger action in the clock input makes the circuit highly tolerant to slower clock rise and fall times.

2. Features and benefits

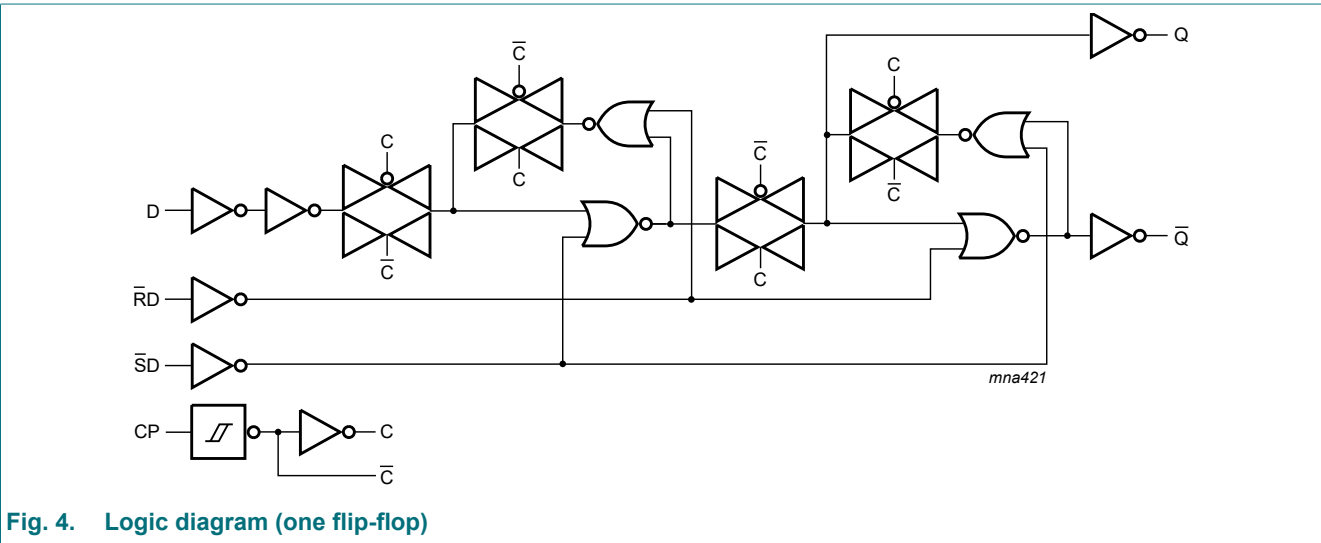
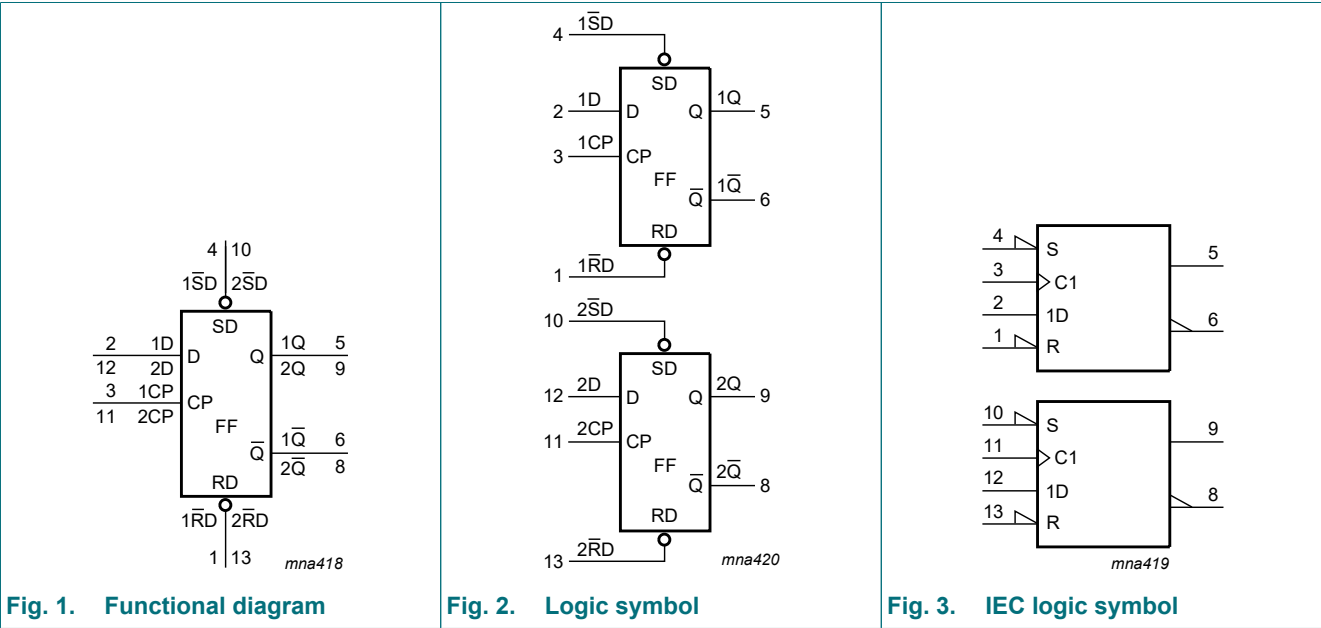
- Balanced propagation delays
- All inputs have Schmitt-trigger actions
- Inputs accept voltages higher than V_{CC}
- Input levels:
 - For 74AHC74: CMOS level
 - For 74AHCT74: TTL level
- ESD protection:
 - HBM EIA/JESD22-A114E exceeds 2000 V
 - MM EIA/JESD22-A115-A exceeds 200 V
 - CDM EIA/JESD22-C101C exceeds 1000 V
- Multiple package options
- Specified from -40 °C to +85 °C and from -40 °C to +125 °C

3. Ordering information

Table 1. Ordering information

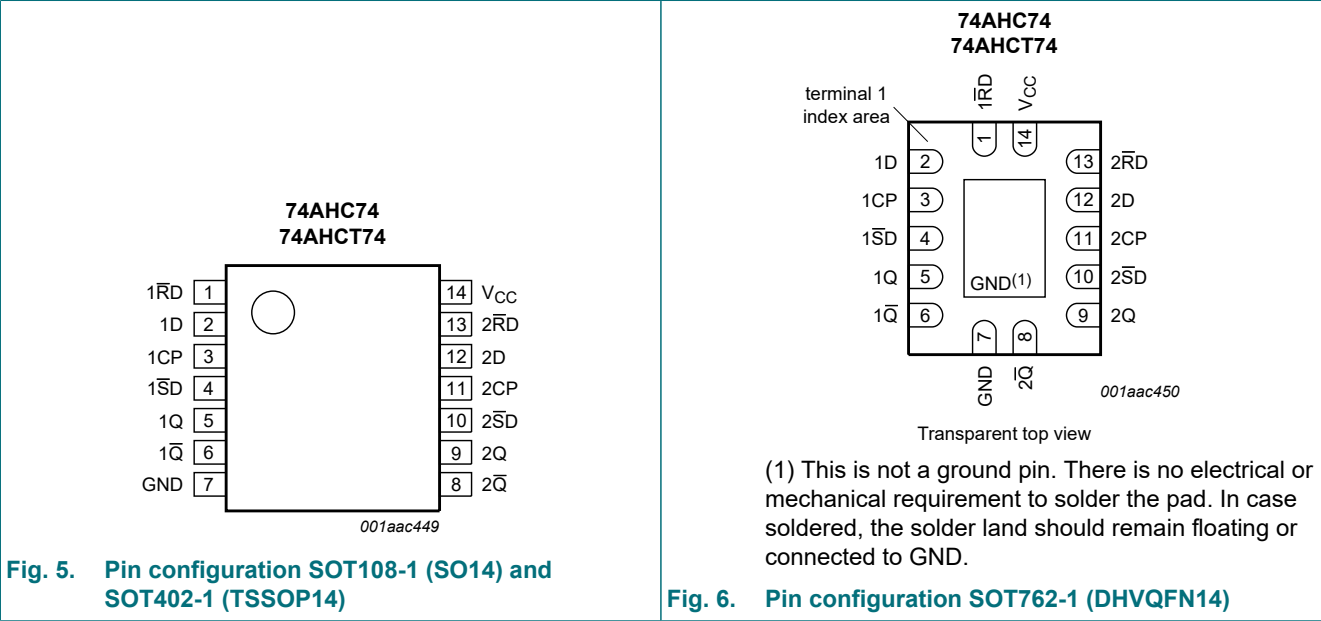
Type number	Package			
	Temperature range	Name	Description	Version
74AHC74D	-40 °C to +125 °C	SO14	plastic small outline package; 14 leads; body width 3.9 mm	SOT108-1
74AHCT74D				
74AHC74PW	-40 °C to +125 °C	TSSOP14	plastic thin shrink small outline package; 14 leads; body width 4.4 mm	SOT402-1
74AHCT74PW				
74AHC74BQ	-40 °C to +125 °C	DHVQFN14	plastic dual in-line compatible thermal enhanced very thin quad flat package; no leads; 14 terminals; body 2.5 × 3 × 0.85 mm	SOT762-1
74AHCT74BQ				

4. Functional diagram



5. Pinning information

5.1. Pinning



5.2. Pin description

Table 2. Pin description

Symbol	Pin	Description
1RD	1	asynchronous reset direct input (active LOW)
1D	2	data input
1CP	3	clock input (LOW to HIGH, edge-triggered)
1SD	4	asynchronous set direct input (active LOW)
1Q	5	true flip-flop output
1Q	6	complement flip-flop output
GND	7	ground (0 V)
2Q	8	complement flip-flop output
2Q	9	true flip-flop output
2SD	10	asynchronous set direct input (active LOW)
2CP	11	clock input (LOW to HIGH, edge-triggered)
2D	12	data input
2RD	13	asynchronous reset direct input (active LOW)
V _{CC}	14	supply voltage

6. Functional description

Table 3. Function table

H = HIGH voltage level; L = LOW voltage level; X = don't care;

↑ = LOW to HIGH transition; Q_{n+1} = state after the next LOW to HIGH CP transition.

Control			Input	Output			
nSD	nRD	nCP	nD	nQ	nQ̄	nQ _{n+1}	nQ̄ _{n+1}
L	H	X	X	H	L	-	-
H	L	X	X	L	H	-	-
L	L	X	X	H	H	-	-
H	H	↑	L	-	-	L	H
H	H	↑	H	-	-	H	L

7. Limiting values

Table 4. Limiting values

In accordance with the Absolute Maximum Rating System (IEC 60134). Voltages are referenced to GND (ground = 0 V).

Symbol	Parameter	Conditions	Min	Max	Unit
V _{CC}	supply voltage		-0.5	+7.0	V
V _I	input voltage		-0.5	+7.0	V
I _{IK}	input clamping current	V _I < -0.5 V [1]	-20	-	mA
I _{OK}	output clamping current	V _O < -0.5 V or V _O > V _{CC} + 0.5 V [1]	-20	+20	mA
I _O	output current	V _O = -0.5 V to (V _{CC} + 0.5 V)	-25	+25	mA
I _{CC}	supply current		-	+75	mA
I _{GND}	ground current		-75	-	mA
T _{stg}	storage temperature		-65	+150	°C
P _{tot}	total power dissipation	T _{amb} = -40 °C to +125 °C [2]	-	500	mW

[1] The input and output voltage ratings may be exceeded if the input and output current ratings are observed.

[2] For SOT108-1 (SO14) package: P_{tot} derates linearly with 10.1 mW/K above 100 °C.

For SOT402-1 (TSSOP14) package: P_{tot} derates linearly with 7.3 mW/K above 81 °C.

For SOT762-1 (DHVQFN14) package: P_{tot} derates linearly with 9.6 mW/K above 98 °C.

8. Recommended operating conditions

Table 5. Operating conditions

Symbol	Parameter	Conditions	74AHC74			74AHCT74			Unit
			Min	Typ	Max	Min	Typ	Max	
V _{CC}	supply voltage		2.0	5.0	5.5	4.5	5.0	5.5	V
V _I	input voltage		0	-	5.5	0	-	5.5	V
V _O	output voltage		0	-	V _{CC}	0	-	V _{CC}	V
T _{amb}	ambient temperature		-40	+25	+125	-40	+25	+125	°C
Δt/ΔV	input transition rise and fall rate	V _{CC} = 3.0 V to 3.6 V	-	-	100	-	-	-	ns/V
		V _{CC} = 4.5 V to 5.5 V	-	-	20	-	-	20	ns/V

9. Static characteristics

Table 6. Static characteristics

At recommended operating conditions; voltages are referenced to GND (ground = 0 V).

Symbol	Parameter	Conditions	25 °C			-40 °C to +85 °C		-40 °C to +125 °C		Unit
			Min	Typ	Max	Min	Max	Min	Max	
74AHC74										
V _{IH}	HIGH-level input voltage	V _{CC} = 2.0 V	1.5	-	-	1.5	-	1.5	-	V
		V _{CC} = 3.0 V	2.1	-	-	2.1	-	2.1	-	V
		V _{CC} = 5.5 V	3.85	-	-	3.85	-	3.85	-	V
V _{IL}	LOW-level input voltage	V _{CC} = 2.0 V	-	-	0.5	-	0.5	-	0.5	V
		V _{CC} = 3.0 V	-	-	0.9	-	0.9	-	0.9	V
		V _{CC} = 5.5 V	-	-	1.65	-	1.65	-	1.65	V
V _{OH}	HIGH-level output voltage	V _I = V _{IH} or V _{IL}								
		I _O = -50 µA; V _{CC} = 2.0 V	1.9	2.0	-	1.9	-	1.9	-	V
		I _O = -50 µA; V _{CC} = 3.0 V	2.9	3.0	-	2.9	-	2.9	-	V
		I _O = -50 µA; V _{CC} = 4.5 V	4.4	4.5	-	4.4	-	4.4	-	V
		I _O = -4.0 mA; V _{CC} = 3.0 V	2.58	-	-	2.48	-	2.40	-	V
		I _O = -8.0 mA; V _{CC} = 4.5 V	3.94	-	-	3.80	-	3.70	-	V
V _{OL}	LOW-level output voltage	V _I = V _{IH} or V _{IL}								
		I _O = 50 µA; V _{CC} = 2.0 V	-	0	0.1	-	0.1	-	0.1	V
		I _O = 50 µA; V _{CC} = 3.0 V	-	0	0.1	-	0.1	-	0.1	V
		I _O = 50 µA; V _{CC} = 4.5 V	-	0	0.1	-	0.1	-	0.1	V
		I _O = 4.0 mA; V _{CC} = 3.0 V	-	-	0.36	-	0.44	-	0.55	V
		I _O = 8.0 mA; V _{CC} = 4.5 V	-	-	0.36	-	0.44	-	0.55	V
I _I	input leakage current	V _I = 5.5 V or GND; V _{CC} = 0 V to 5.5 V	-	-	0.1	-	1.0	-	2.0	µA
I _{CC}	supply current	V _I = V _{CC} or GND; I _O = 0 A; V _{CC} = 5.5 V	-	-	2.0	-	20	-	40	µA
C _I	input capacitance	V _I = V _{CC} or GND	-	3	10	-	10	-	10	pF
74AHCT74										
V _{IH}	HIGH-level input voltage	V _{CC} = 4.5 V to 5.5 V	2.0	-	-	2.0	-	2.0	-	V
V _{IL}	LOW-level input voltage	V _{CC} = 4.5 V to 5.5 V	-	-	0.8	-	0.8	-	0.8	V
V _{OH}	HIGH-level output voltage	V _I = V _{IH} or V _{IL} ; V _{CC} = 4.5 V								
		I _O = -50 µA	4.4	4.5	-	4.4	-	4.4	-	V
		I _O = -8.0 mA	3.94	-	-	3.80	-	3.70	-	V
V _{OL}	LOW-level output voltage	V _I = V _{IH} or V _{IL} ; V _{CC} = 4.5 V								
		I _O = 50 µA	-	0	0.1	-	0.1	-	0.1	V
		I _O = 8.0 mA	-	-	0.36	-	0.44	-	0.55	V
I _I	input leakage current	V _I = 5.5 V or GND; V _{CC} = 0 V to 5.5 V	-	-	0.1	-	1.0	-	2.0	µA
I _{CC}	supply current	V _I = V _{CC} or GND; I _O = 0 A; V _{CC} = 5.5 V	-	-	2.0	-	20	-	40	µA

Dual D-type flip-flop with set and reset; positive-edge trigger

Symbol	Parameter	Conditions	25 °C			-40 °C to +85 °C		-40 °C to +125 °C		Unit
			Min	Typ	Max	Min	Max	Min	Max	
ΔI_{CC}	additional supply current	per input pin; $V_I = V_{CC} - 2.1\text{ V}$; other pins at V_{CC} or GND; $I_O = 0\text{ A}$; $V_{CC} = 4.5\text{ V}$ to 5.5 V	-	-	1.35	-	1.5	-	1.5	mA
C_I	input capacitance	$V_I = V_{CC}$ or GND	-	3	10	-	10	-	10	pF

10. Dynamic characteristics

Table 7. Dynamic characteristics

Voltages are referenced to GND (ground = 0 V); for test circuit, see Fig. 9.

Symbol	Parameter	Conditions	25 °C			-40 °C to +85 °C		-40 °C to +125 °C		Unit
			Min	Typ [1]	Max	Min	Max	Min	Max	
74AHC74										
t _{pd}	propagation delay	nCP to nQ, nQ̄; see Fig. 7 [2]								
		V _{CC} = 3.0 V to 3.6 V; C _L = 15 pF	-	5.2	11.9	1.0	14.0	1.0	15.0	ns
		V _{CC} = 3.0 V to 3.6 V; C _L = 50 pF	-	7.4	15.4	1.0	17.5	1.0	19.5	ns
		V _{CC} = 4.5 V to 5.5 V; C _L = 15 pF	-	3.7	7.3	1.0	8.5	1.0	9.5	ns
		V _{CC} = 4.5 V to 5.5 V; C _L = 50 pF	-	5.2	9.3	1.0	10.5	1.0	12.0	ns
		nSD, nRD to nQ, nQ̄; see Fig. 8								
		V _{CC} = 3.0 V to 3.6 V; C _L = 15 pF	-	5.4	12.3	1.0	14.5	1.0	15.5	ns
		V _{CC} = 3.0 V to 3.6 V; C _L = 50 pF	-	7.7	15.8	1.0	18.0	1.0	20.0	ns
		V _{CC} = 4.5 V to 5.5 V; C _L = 15 pF	-	3.7	7.7	1.0	9.0	1.0	10.0	ns
		V _{CC} = 4.5 V to 5.5 V; C _L = 50 pF	-	5.3	9.7	1.0	11.0	1.0	12.5	ns
f _{max}	maximum frequency	see Fig. 7								
		V _{CC} = 3.0 V to 3.6 V; C _L = 15 pF	80	125	-	70	-	70	-	MHz
		V _{CC} = 3.0 V to 3.6 V; C _L = 50 pF	50	75	-	45	-	45	-	MHz
		V _{CC} = 4.5 V to 5.5 V; C _L = 15 pF	130	170	-	110	-	110	-	MHz
		V _{CC} = 4.5 V to 5.5 V; C _L = 50 pF	90	115	-	75	-	75	-	MHz
t _w	pulse width	CP HIGH or LOW; nSD, nRD LOW; see Fig. 7 and Fig. 8								
		V _{CC} = 3.0 V to 3.6 V	6.0	-	-	7.0	-	7.0	-	ns
		V _{CC} = 4.5 V to 5.5 V	5.0	-	-	5.0	-	5.0	-	ns
t _{su}	set-up time	nD to nCP; see Fig. 7								
		V _{CC} = 3.0 V to 3.6 V	6.0	-	-	7.0	-	7.0	-	ns
		V _{CC} = 4.5 V to 5.5 V	5.0	-	-	5.0	-	5.0	-	ns
t _h	hold time	nD to nCP; see Fig. 7								
		V _{CC} = 3.0 V to 3.6 V	0.5	-	-	0.5	-	0.5	-	ns
		V _{CC} = 4.5 V to 5.5 V	0.5	-	-	0.5	-	0.5	-	ns

Dual D-type flip-flop with set and reset; positive-edge trigger

Symbol	Parameter	Conditions	25 °C			-40 °C to +85 °C		-40 °C to +125 °C		Unit
			Min	Typ [1]	Max	Min	Max	Min	Max	
t_{rec}	recovery time	nRD to nCP; see Fig. 8								
		$V_{\text{CC}} = 3.0 \text{ V to } 3.6 \text{ V}$	5.0	-	-	5.0	-	5.0	-	ns
		$V_{\text{CC}} = 4.5 \text{ V to } 5.5 \text{ V}$	3.0	-	-	3.0	-	3.0	-	ns
C_{PD}	power dissipation capacitance	$f_i = 1 \text{ MHz}$; $V_i = \text{GND to } V_{\text{CC}}$ [3]	-	12	-	-	-	-	-	pF
74AHCT74										
t_{pd}	propagation delay	nCP to nQ, n \bar{Q} ; see Fig. 7 [2]								
		$V_{\text{CC}} = 4.5 \text{ V to } 5.5 \text{ V}$; $C_L = 15 \text{ pF}$	-	3.3	7.8	1.0	9.0	1.0	10.0	ns
		$V_{\text{CC}} = 4.5 \text{ V to } 5.5 \text{ V}$; $C_L = 50 \text{ pF}$	-	4.8	8.8	1.0	10.0	1.0	11.0	ns
		n \bar{S} D, n \bar{R} D to nQ, n \bar{Q} ; see Fig. 8								
		$V_{\text{CC}} = 4.5 \text{ V to } 5.5 \text{ V}$; $C_L = 15 \text{ pF}$	-	3.7	10.4	1.0	12.0	1.0	13.0	ns
		$V_{\text{CC}} = 4.5 \text{ V to } 5.5 \text{ V}$; $C_L = 50 \text{ pF}$	-	5.3	11.4	1.0	13.0	1.0	14.5	ns
f_{max}	maximum frequency	see Fig. 7								
		$V_{\text{CC}} = 4.5 \text{ V to } 5.5 \text{ V}$; $C_L = 15 \text{ pF}$	100	160	-	80	-	80	-	MHz
		$V_{\text{CC}} = 4.5 \text{ V to } 5.5 \text{ V}$; $C_L = 50 \text{ pF}$	80	140	-	65	-	65	-	MHz
t_W	pulse width	CP HIGH or LOW; n \bar{S} D, n \bar{R} D LOW; $V_{\text{CC}} = 4.5 \text{ V to } 5.5 \text{ V}$; see Fig. 7 and Fig. 8	5.0	-	-	5.0	-	5.0	-	ns
t_{su}	set-up time	nD to nCP; $V_{\text{CC}} = 4.5 \text{ V to } 5.5 \text{ V}$; see Fig. 7	5.0	-	-	5.0	-	5.0	-	ns
t_h	hold time	nD to nCP; $V_{\text{CC}} = 4.5 \text{ V to } 5.5 \text{ V}$; see Fig. 7	0	-	-	0	-	0	-	ns
t_{rec}	recovery time	nRD to nCP; $V_{\text{CC}} = 4.5 \text{ V to } 5.5 \text{ V}$; see Fig. 8	3.5	-	-	3.5	-	3.5	-	ns
C_{PD}	power dissipation capacitance	$f_i = 1 \text{ MHz}$; $V_i = \text{GND to } V_{\text{CC}}$ [3]	-	16	-	-	-	-	-	pF

[1] Typical values are measured at nominal supply voltage ($V_{\text{CC}} = 3.3 \text{ V}$ and $V_{\text{CC}} = 5.0 \text{ V}$).

[2] t_{pd} is the same as t_{PLH} and t_{PHL} .

[3] C_{PD} is used to determine the dynamic power dissipation (P_D in μW).

$$P_D = C_{\text{PD}} \times V_{\text{CC}}^2 \times f_i \times N + \Sigma(C_L \times V_{\text{CC}}^2 \times f_o) \text{ where:}$$

f_i = input frequency in MHz;

f_o = output frequency in MHz;

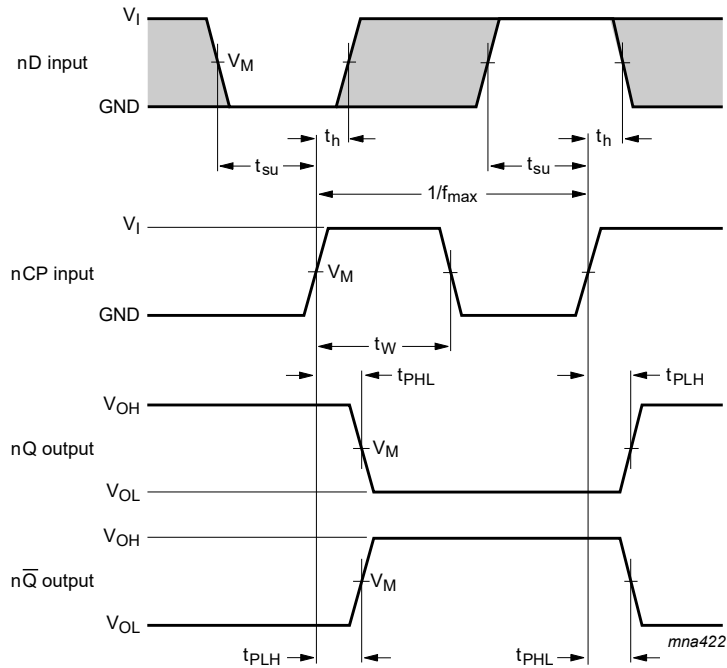
C_L = output load capacitance in pF;

V_{CC} = supply voltage in V;

N = number of inputs switching;

$\Sigma(C_L \times V_{\text{CC}}^2 \times f_o)$ = sum of the outputs.

10.1. Waveforms

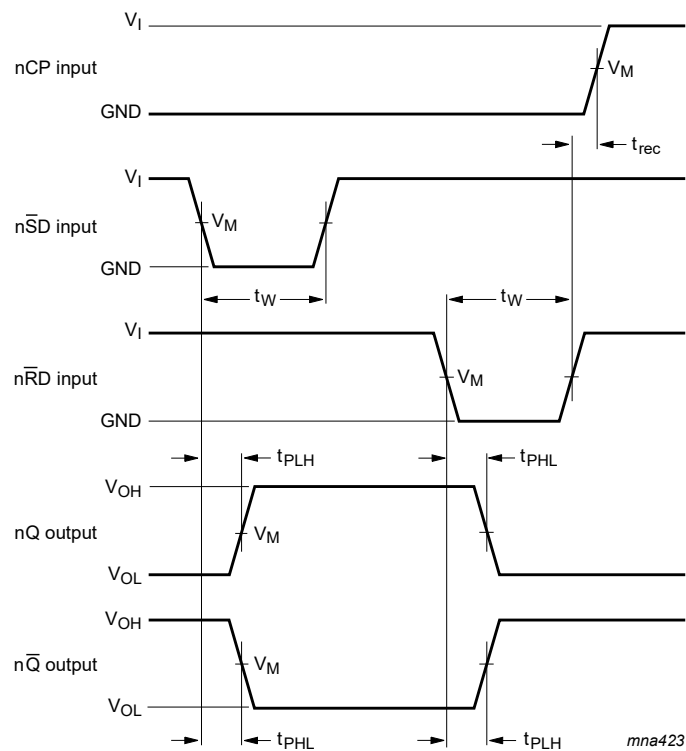


Measurement points are given in [Table 8](#).

The shaded areas indicate when the input is permitted to change for predictable output performance.

V_{OL} and V_{OH} are typical voltage output levels that occur with the output load.

Fig. 7. Clock pulse width, maximum frequency, set-up times, hold times and input to output propagation delays



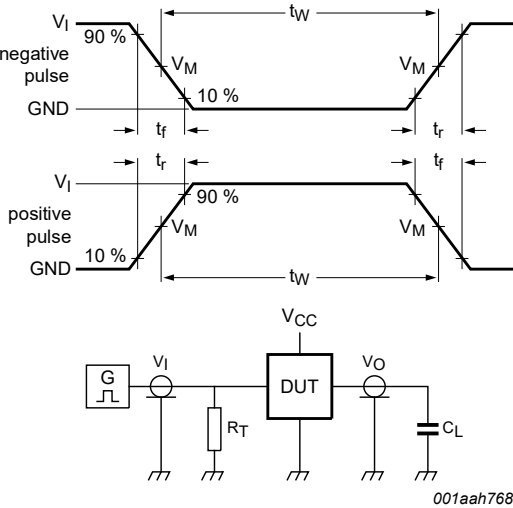
Measurement points are given in [Table 8](#).

V_{OL} and V_{OH} are typical voltage output levels that occur with the output load.

Fig. 8. Set and reset pulse widths, recovery time and input to output propagation delays

Table 8. Measurement points

Type	Input		Output
	V_M		V_M
74AHC74	$0.5 \times V_{CC}$		$0.5 \times V_{CC}$
74AHCT74	1.5 V		$0.5 \times V_{CC}$



For test data, see [Table 9](#).
Definitions for test circuit:
 C_L = Load capacitance including jig and probe capacitance.
 R_T = Termination resistance should be equal to output impedance Z_o of the pulse generator.

Fig. 9. Test circuit for measuring switching times

Table 9. Test data

Type	Input		Load	Test
	V_I	t_r, t_f	C_L	
74AHC74	V_{CC}	$\leq 3.0 \text{ ns}$	50 pF, 15 pF	t_{PLH}, t_{PHL}
74AHCT74	3.0 V	$\leq 3.0 \text{ ns}$	50 pF, 15 pF	t_{PLH}, t_{PHL}

11. Package outline

SO14: plastic small outline package; 14 leads; body width 3.9 mm

SOT108-1

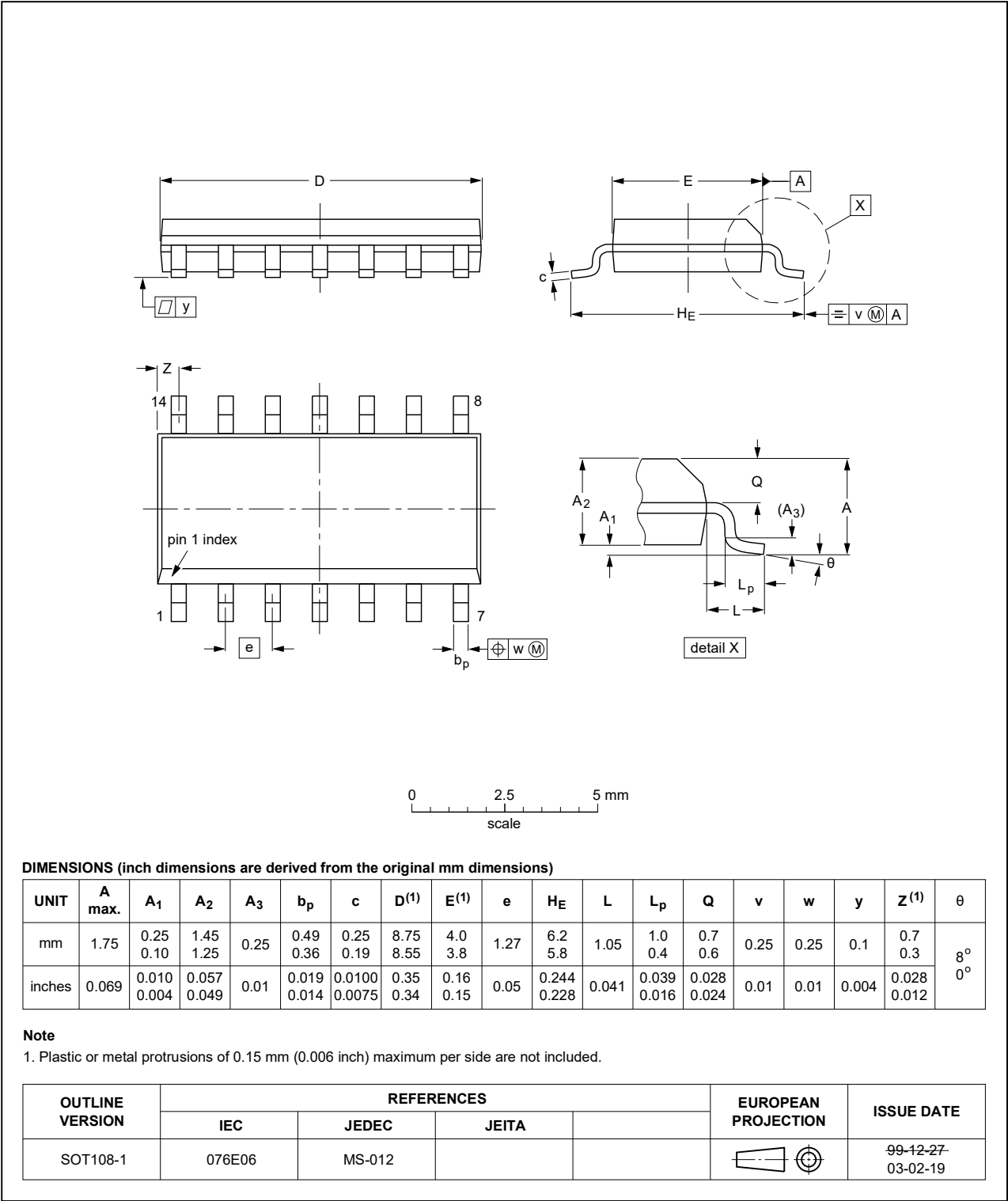


Fig. 10. Package outline SOT108-1 (SO14)

TSSOP14: plastic thin shrink small outline package; 14 leads; body width 4.4 mm

SOT402-1

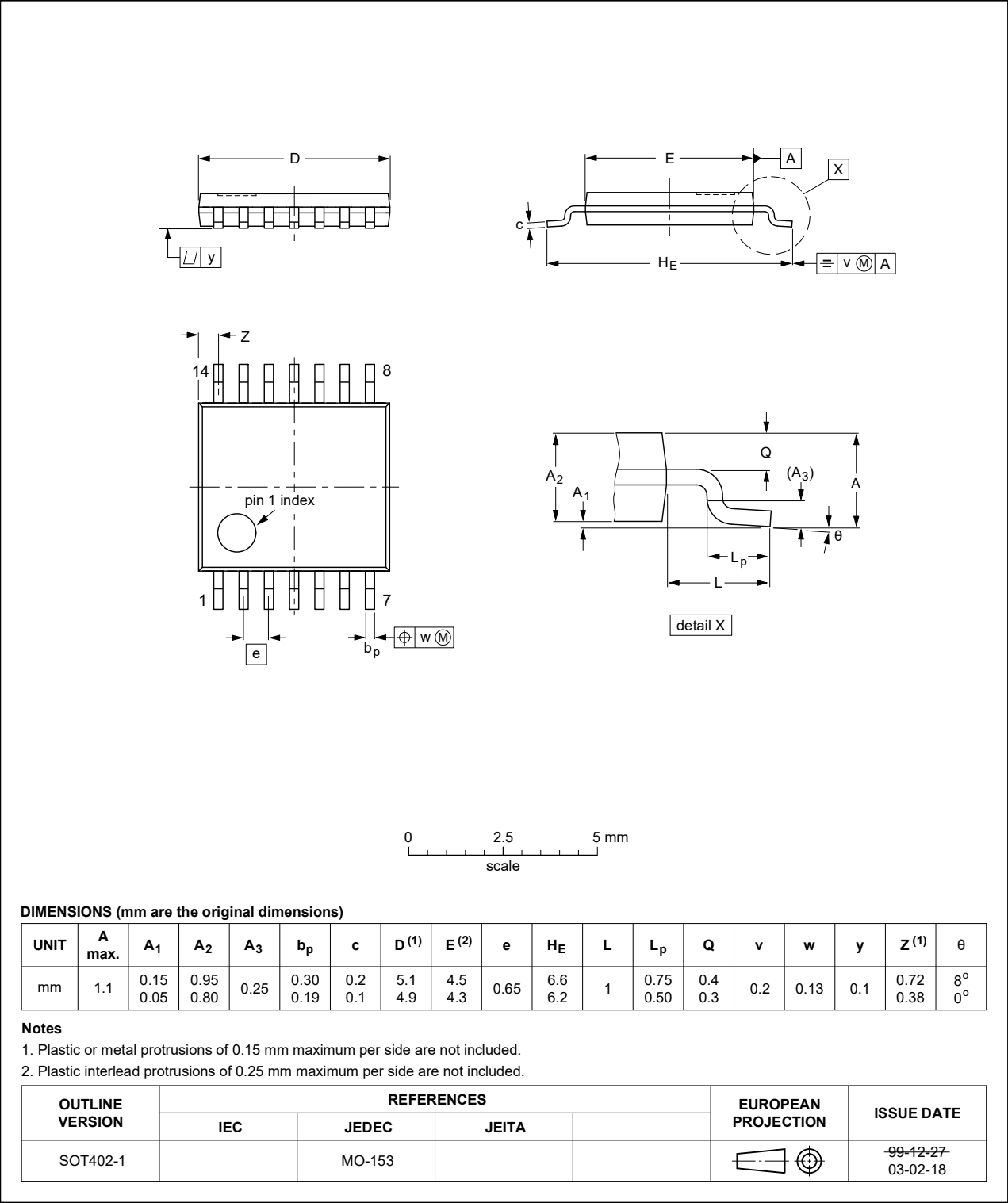
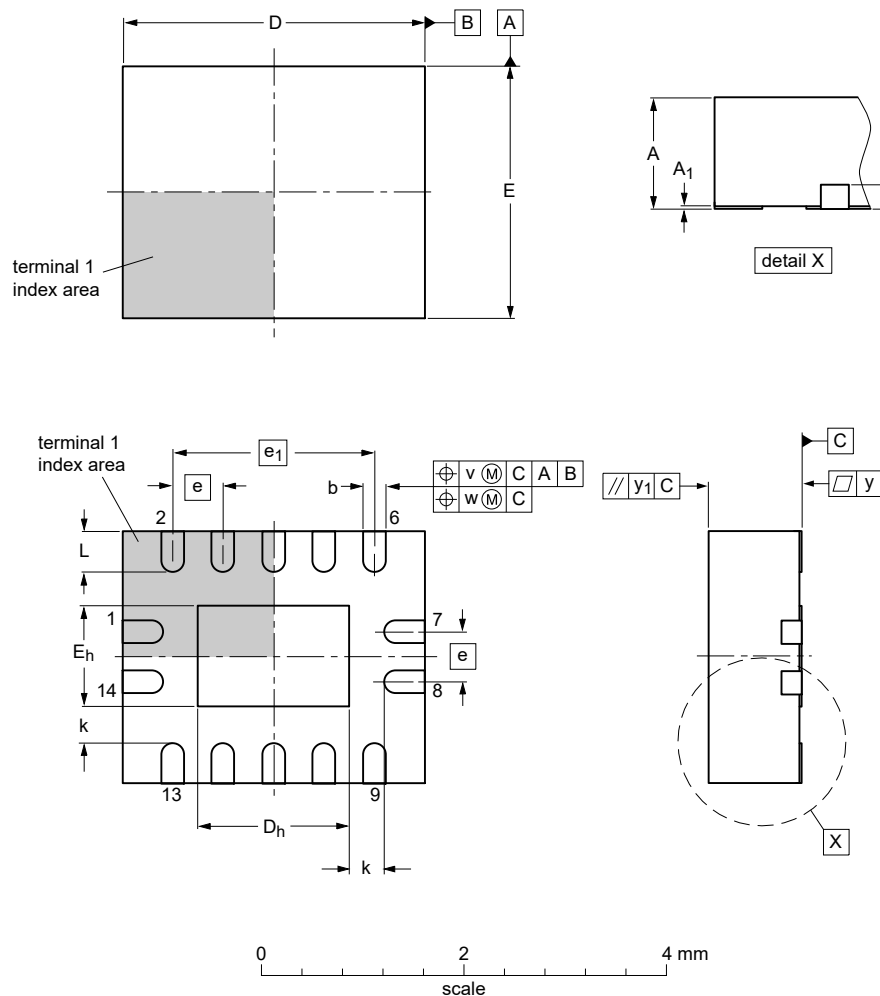


Fig. 11. Package outline SOT402-1 (TSSOP14)

DHVQFN14: plastic dual in-line compatible thermal enhanced very thin quad flat package; no leads; 14 terminals; body 2.5 x 3 x 0.85 mm

SOT762-1



Dimensions (mm are the original dimensions)

Unit		A ⁽¹⁾	A ₁	b	c	D ⁽¹⁾	D _h	E ⁽¹⁾	E _h	e	e ₁	k	L	v	w	y	y ₁
mm	max	1	0.05	0.30		3.1	1.65	2.6	1.15				0.5				
	nom		0.02	0.25	0.2	3.0	1.50	2.5	1.00	0.5	2		0.4	0.1	0.05	0.05	0.1
	min		0.00	0.18		2.9	1.35	2.4	0.85			0.2	0.3				

Note

1. Plastic or metal protrusions of 0.075 mm maximum per side are not included.

sot762-1_po


Outline version	References				European projection	Issue date
	IEC	JEDEC	JEITA			
SOT762-1		MO-241				15-04-10 15-05-05

Fig. 12. Package outline SOT762-1 (DHVQFN14)

12. Abbreviations

Table 10. Abbreviations

Acronym	Description
CDM	Charged Device Model
CMOS	Complementary Metal-Oxide Semiconductor
ESD	ElectroStatic Discharge
HBM	Human Body Model
LSTTL	Low-power Schottky Transistor-Transistor Logic
MM	Machine Model

13. Revision history

Table 11. Revision history

Document ID	Release date	Data sheet status	Change notice	Supersedes
74AHC_AHCT74 v.8	20200422	Product data sheet	-	74AHC_AHCT74 v.7
Modifications:	<ul style="list-style-type: none"> The format of this data sheet has been redesigned to comply with the identity guidelines of Nexperia. Legal texts have been adapted to the new company name where appropriate. Section 5.1: Corrected pin configuration drawings (errata). Table 4: Derating values for P_{tot} total power dissipation updated. Fig. 12: Package outline drawing SOT762-1 (DHVQFN14) updated. 			
74AHC_AHCT74 v.7	20150421	Product data sheet	-	74AHC_AHCT74 v.6
Modifications:	<ul style="list-style-type: none"> Table 7: minimum f_{max} values at 3.0 V to 3.6 V for 74AHC74 corrected (errata). 			
74AHC_AHCT74 v.6	20141020	Product data sheet	-	74AHC_AHCT74 v.5
Modifications:	<ul style="list-style-type: none"> Table 3 corrected (errata). 			
74AHC_AHCT74 v.5	20080609	Product data sheet	-	74AHC_AHCT74 v.4
Modifications:	<ul style="list-style-type: none"> The format of this data sheet has been redesigned to comply with the new identity guidelines of NXP Semiconductors. Legal texts have been adapted to the new company name where appropriate. Table 6: the conditions for input leakage current have been changed. 			
74AHC_AHCT74 v.4	20050207	Product data sheet	-	74AHC_AHCT74 v.3
74AHC_AHCT74 v.3	20040429	Product specification	-	74AHC_AHCT74 v.2
74AHC_AHCT74 v.2	19990923	Product specification	-	74AHC_AHCT74 v.1
74AHC_AHCT74 v.1	19990805	Product specification	-	-

14. Legal information

Data sheet status

Document status [1][2]	Product status [3]	Definition
Objective [short] data sheet	Development	This document contains data from the objective specification for product development.
Preliminary [short] data sheet	Qualification	This document contains data from the preliminary specification.
Product [short] data sheet	Production	This document contains the product specification.

- [1] Please consult the most recently issued document before initiating or completing a design.
- [2] The term 'short data sheet' is explained in section "Definitions".
- [3] The product status of device(s) described in this document may have changed since this document was published and may differ in case of multiple devices. The latest product status information is available on the internet at <https://www.nexperia.com>.

Definitions

Draft — The document is a draft version only. The content is still under internal review and subject to formal approval, which may result in modifications or additions. Nexperia does not give any representations or warranties as to the accuracy or completeness of information included herein and shall have no liability for the consequences of use of such information.

Short data sheet — A short data sheet is an extract from a full data sheet with the same product type number(s) and title. A short data sheet is intended for quick reference only and should not be relied upon to contain detailed and full information. For detailed and full information see the relevant full data sheet, which is available on request via the local Nexperia sales office. In case of any inconsistency or conflict with the short data sheet, the full data sheet shall prevail.

Product specification — The information and data provided in a Product data sheet shall define the specification of the product as agreed between Nexperia and its customer, unless Nexperia and customer have explicitly agreed otherwise in writing. In no event however, shall an agreement be valid in which the Nexperia product is deemed to offer functions and qualities beyond those described in the Product data sheet.

Disclaimers

Limited warranty and liability — Information in this document is believed to be accurate and reliable. However, Nexperia does not give any representations or warranties, expressed or implied, as to the accuracy or completeness of such information and shall have no liability for the consequences of use of such information. Nexperia takes no responsibility for the content in this document if provided by an information source outside of Nexperia.

In no event shall Nexperia be liable for any indirect, incidental, punitive, special or consequential damages (including - without limitation - lost profits, lost savings, business interruption, costs related to the removal or replacement of any products or rework charges) whether or not such damages are based on tort (including negligence), warranty, breach of contract or any other legal theory.

Notwithstanding any damages that customer might incur for any reason whatsoever, Nexperia's aggregate and cumulative liability towards customer for the products described herein shall be limited in accordance with the Terms and conditions of commercial sale of Nexperia.

Right to make changes — Nexperia reserves the right to make changes to information published in this document, including without limitation specifications and product descriptions, at any time and without notice. This document supersedes and replaces all information supplied prior to the publication hereof.

Suitability for use — Nexperia products are not designed, authorized or warranted to be suitable for use in life support, life-critical or safety-critical systems or equipment, nor in applications where failure or malfunction of an Nexperia product can reasonably be expected to result in personal

injury, death or severe property or environmental damage. Nexperia and its suppliers accept no liability for inclusion and/or use of Nexperia products in such equipment or applications and therefore such inclusion and/or use is at the customer's own risk.

Quick reference data — The Quick reference data is an extract of the product data given in the Limiting values and Characteristics sections of this document, and as such is not complete, exhaustive or legally binding.

Applications — Applications that are described herein for any of these products are for illustrative purposes only. Nexperia makes no representation or warranty that such applications will be suitable for the specified use without further testing or modification.

Customers are responsible for the design and operation of their applications and products using Nexperia products, and Nexperia accepts no liability for any assistance with applications or customer product design. It is customer's sole responsibility to determine whether the Nexperia product is suitable and fit for the customer's applications and products planned, as well as for the planned application and use of customer's third party customer(s). Customers should provide appropriate design and operating safeguards to minimize the risks associated with their applications and products.

Nexperia does not accept any liability related to any default, damage, costs or problem which is based on any weakness or default in the customer's applications or products, or the application or use by customer's third party customer(s). Customer is responsible for doing all necessary testing for the customer's applications and products using Nexperia products in order to avoid a default of the applications and the products or of the application or use by customer's third party customer(s). Nexperia does not accept any liability in this respect.

Limiting values — Stress above one or more limiting values (as defined in the Absolute Maximum Ratings System of IEC 60134) will cause permanent damage to the device. Limiting values are stress ratings only and (proper) operation of the device at these or any other conditions above those given in the Recommended operating conditions section (if present) or the Characteristics sections of this document is not warranted. Constant or repeated exposure to limiting values will permanently and irreversibly affect the quality and reliability of the device.

Terms and conditions of commercial sale — Nexperia products are sold subject to the general terms and conditions of commercial sale, as published at <http://www.nexperia.com/profile/terms>, unless otherwise agreed in a valid written individual agreement. In case an individual agreement is concluded only the terms and conditions of the respective agreement shall apply. Nexperia hereby expressly objects to applying the customer's general terms and conditions with regard to the purchase of Nexperia products by customer.

No offer to sell or license — Nothing in this document may be interpreted or construed as an offer to sell products that is open for acceptance or the grant, conveyance or implication of any license under any copyrights, patents or other industrial or intellectual property rights.

Export control — This document as well as the item(s) described herein may be subject to export control regulations. Export might require a prior authorization from competent authorities.

Non-automotive qualified products — Unless this data sheet expressly states that this specific Nexperia product is automotive qualified, the product is not suitable for automotive use. It is neither qualified nor tested in accordance with automotive testing or application requirements. Nexperia accepts no liability for inclusion and/or use of non-automotive qualified products in automotive equipment or applications.

In the event that customer uses the product for design-in and use in automotive applications to automotive specifications and standards, customer (a) shall use the product without Nexperia's warranty of the product for such automotive applications, use and specifications, and (b) whenever customer uses the product for automotive applications beyond Nexperia's specifications such use shall be solely at customer's own risk, and (c) customer fully indemnifies Nexperia for any liability, damages or failed product claims resulting from customer design and use of the product for automotive applications beyond Nexperia's standard warranty and Nexperia's product specifications.

Translations — A non-English (translated) version of a document is for reference only. The English version shall prevail in case of any discrepancy between the translated and English versions.

Trademarks

Notice: All referenced brands, product names, service names and trademarks are the property of their respective owners.

Contents

1. General description.....	1
2. Features and benefits.....	1
3. Ordering information.....	1
4. Functional diagram.....	2
5. Pinning information.....	3
5.1. Pinning.....	3
5.2. Pin description.....	3
6. Functional description.....	4
7. Limiting values.....	4
8. Recommended operating conditions.....	4
9. Static characteristics.....	5
10. Dynamic characteristics.....	6
10.1. Waveforms.....	8
11. Package outline.....	10
12. Abbreviations.....	13
13. Revision history.....	13
14. Legal information.....	14

© Nexperia B.V. 2020. All rights reserved

For more information, please visit: <http://www.nexperia.com>

For sales office addresses, please send an email to: salesaddresses@nexperia.com

Date of release: 22 April 2020